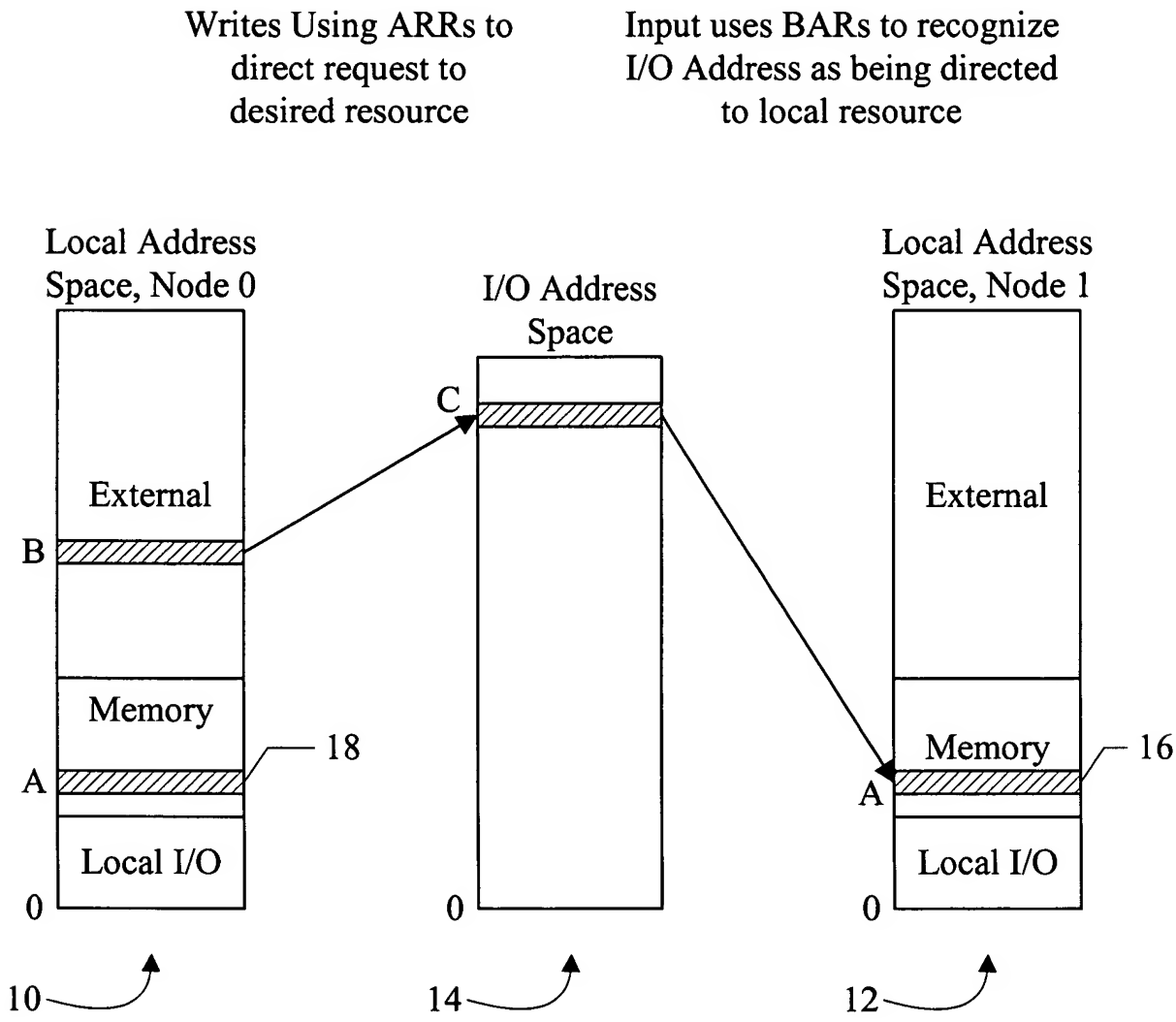

Fig. 1A
(Prior Art)

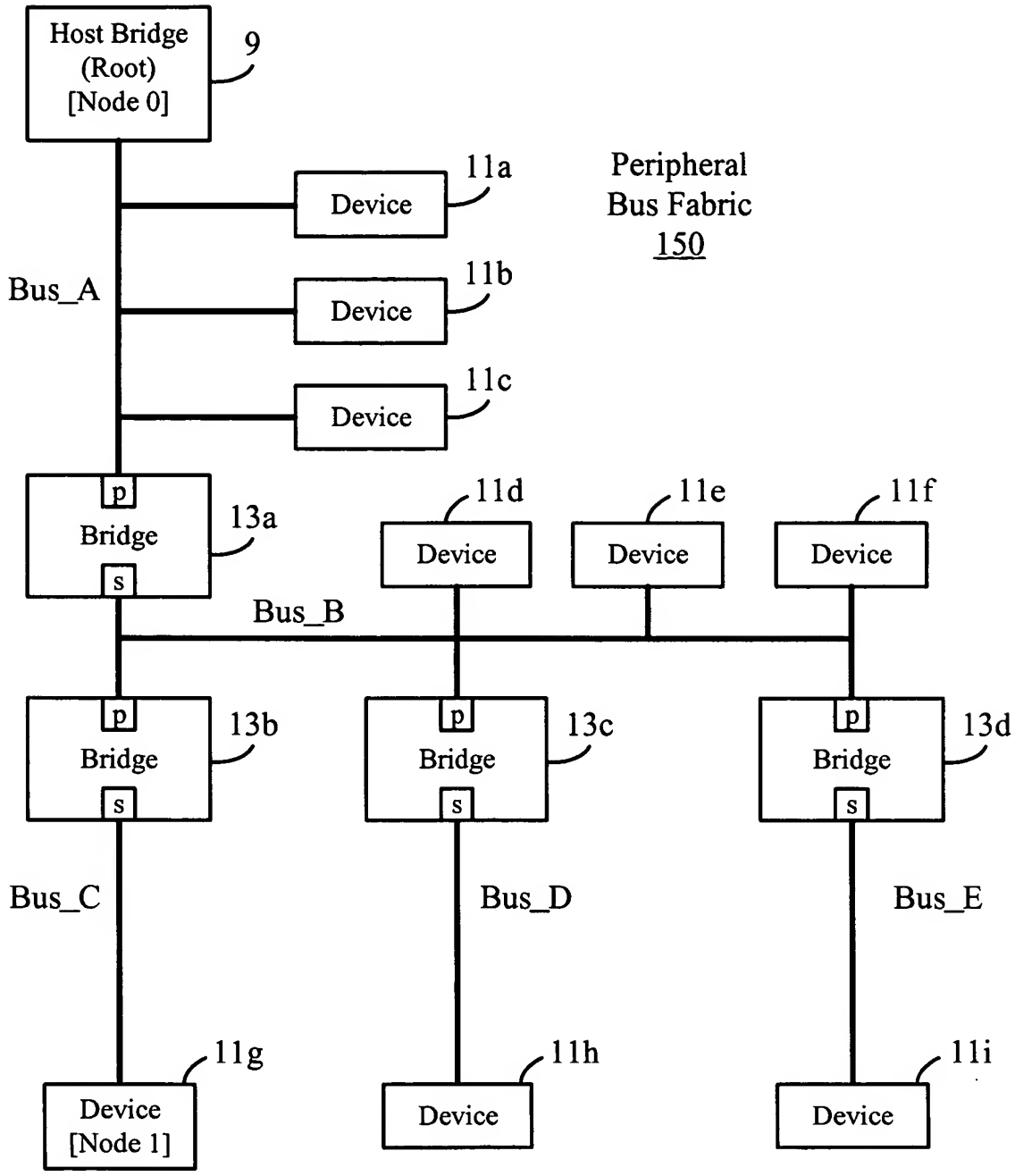

Fig. 1B
(Prior Art)

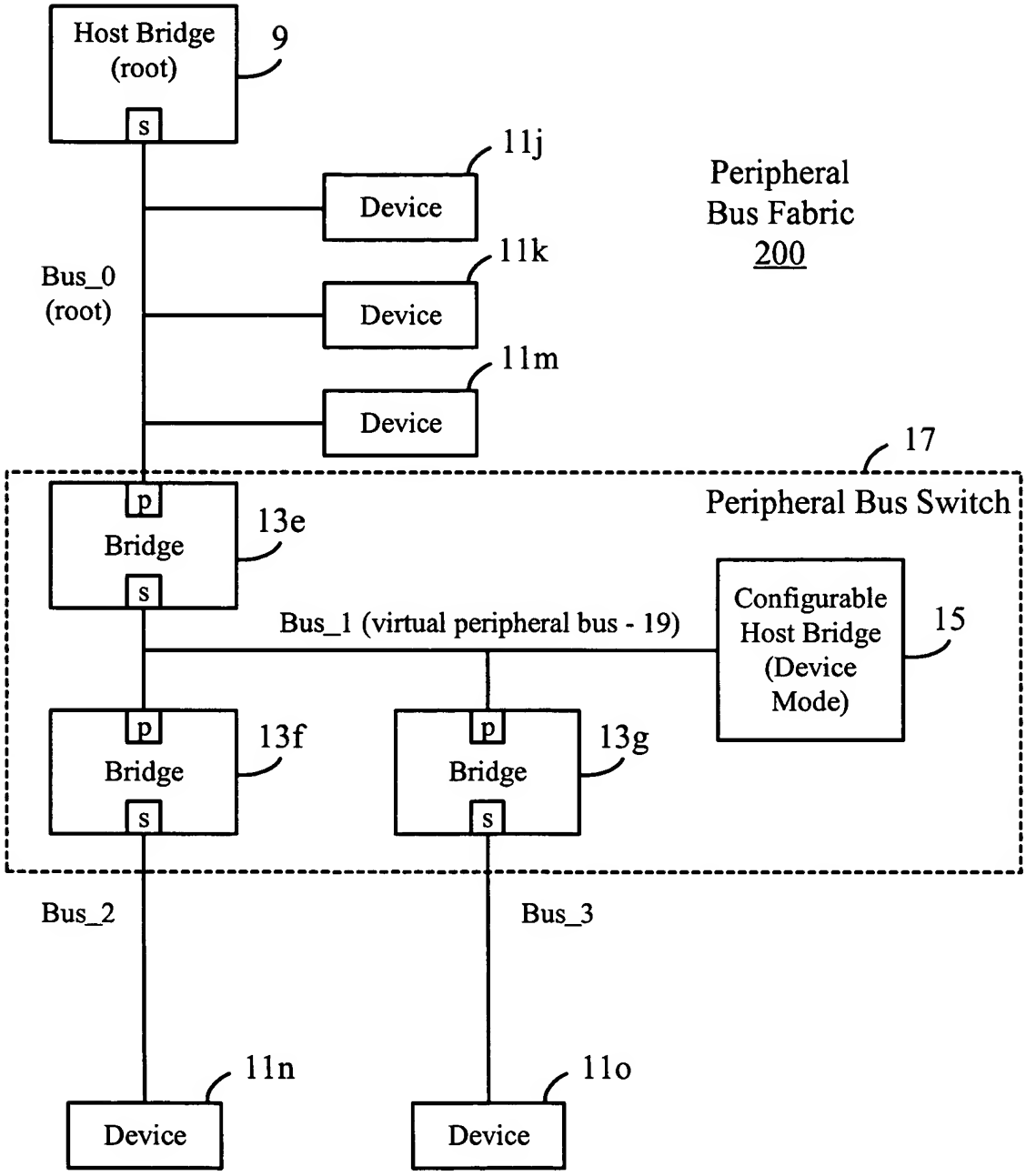
Host Bridge
(root)
9
s
11j
Device
Peripheral
Bus Fabric
200
11k
Bus_0
(root)
Device
11m
Device
17
Peripheral Bus Switch
p
Bridge
13e
s
Bus_1 (virtual peripheral bus - 19)
Configurable
Host Bridge
(Device
Mode)
15
p
Bridge
13f
s
p
Bridge
13g
s
Bus_2
Bus_3
11n
11o
Device
Device

Fig. 2A

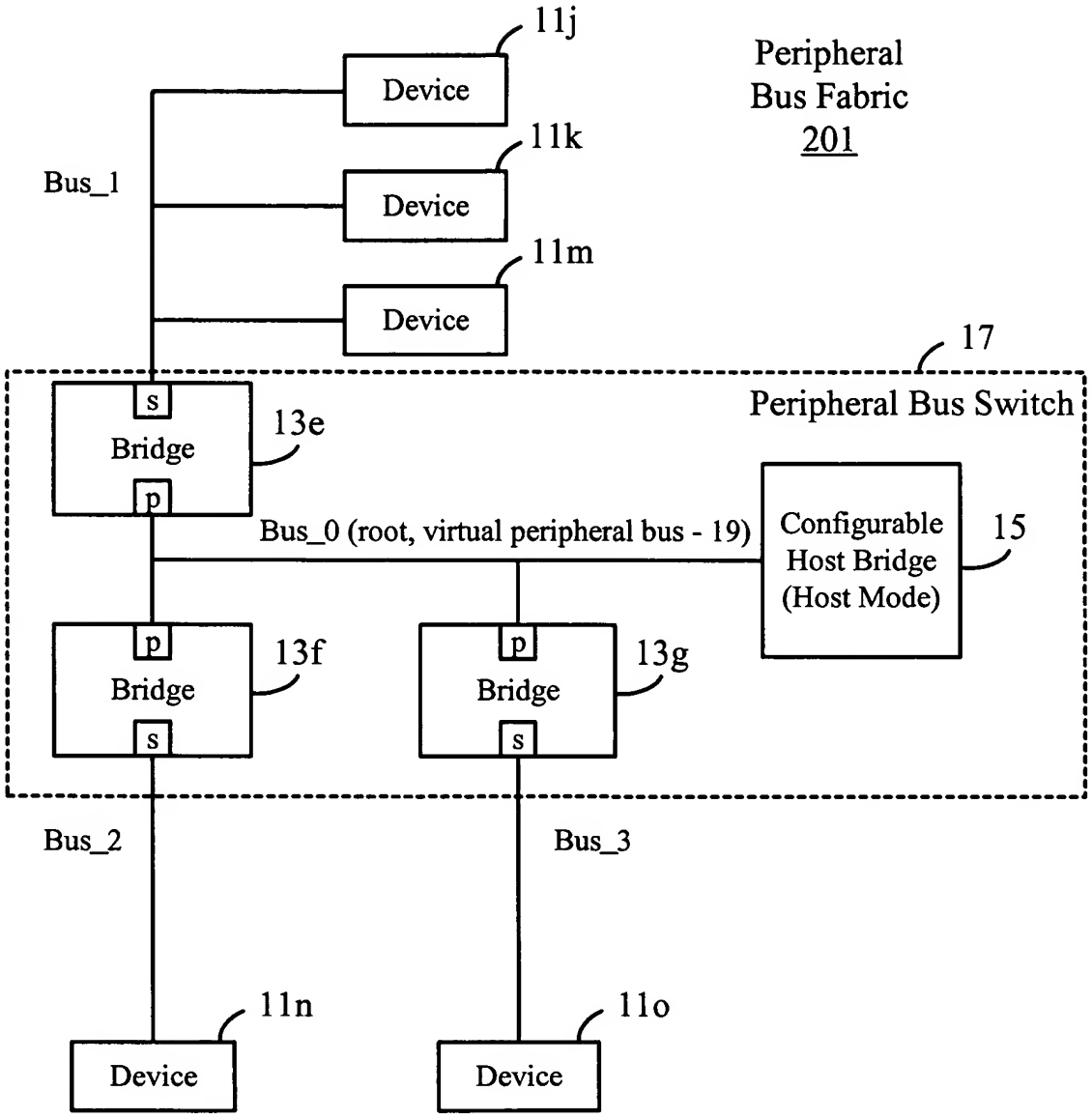
11j
Device
Peripheral
Bus Fabric
201
11k
Bus_1
Device
11m
Device
17
Peripheral Bus Switch
s
Bridge
13e
p
Bus_0 (root, virtual peripheral bus - 19)
Configurable
Host Bridge
(Host Mode)
15
p
Bridge
13f
s
p
Bridge
13g
s
Bus_2
Bus_3
11n
11o
Device
Device

Fig. 2B

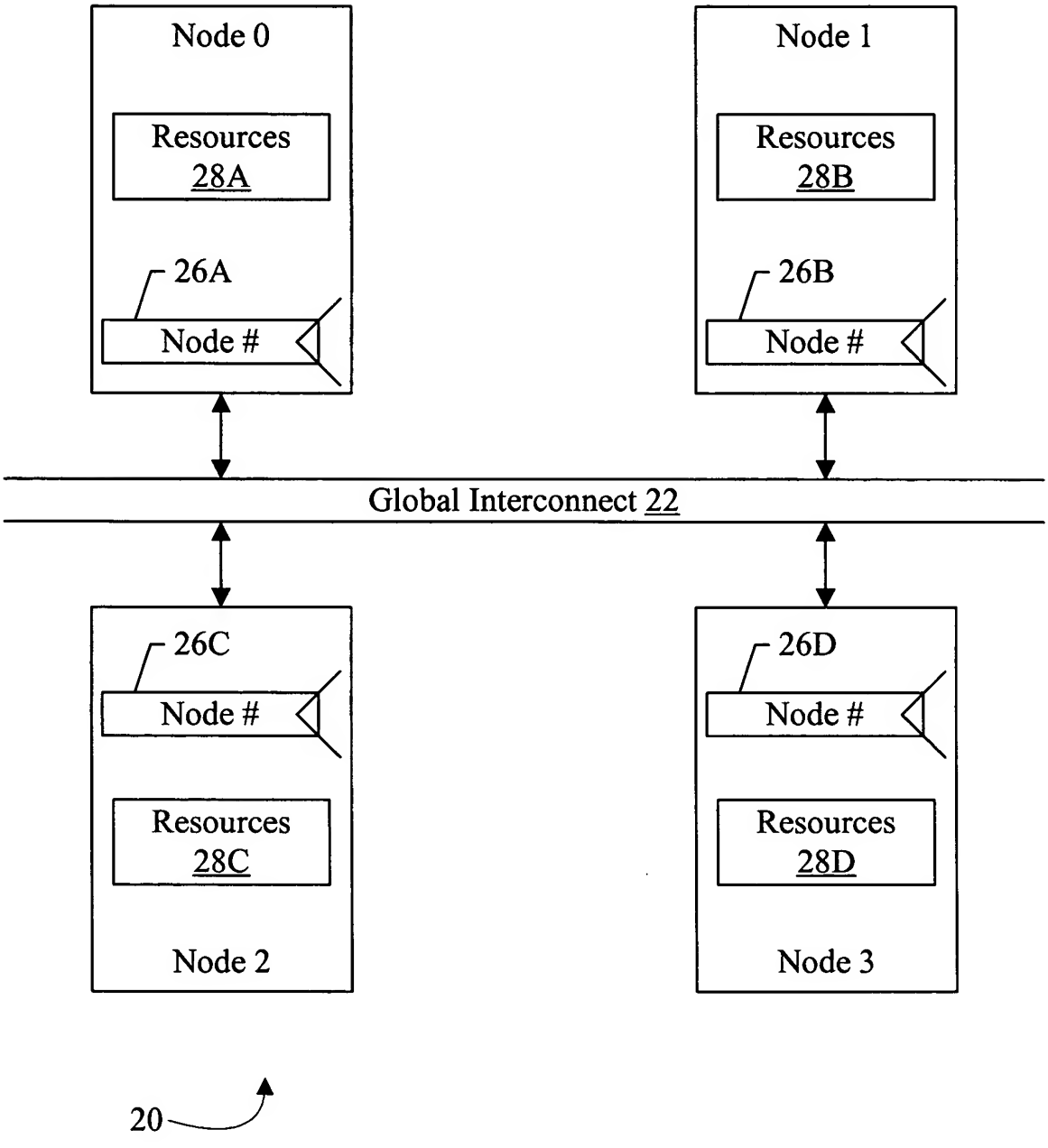
Node 0
Resources
28A
26A
Node #
Node 1
Resources
28B
26B
Node #
Global Interconnect 22
26C
Node #
Resources
28C
Node 2
26D
Node #
Resources
28D
Node 3
20

Fig. 2C

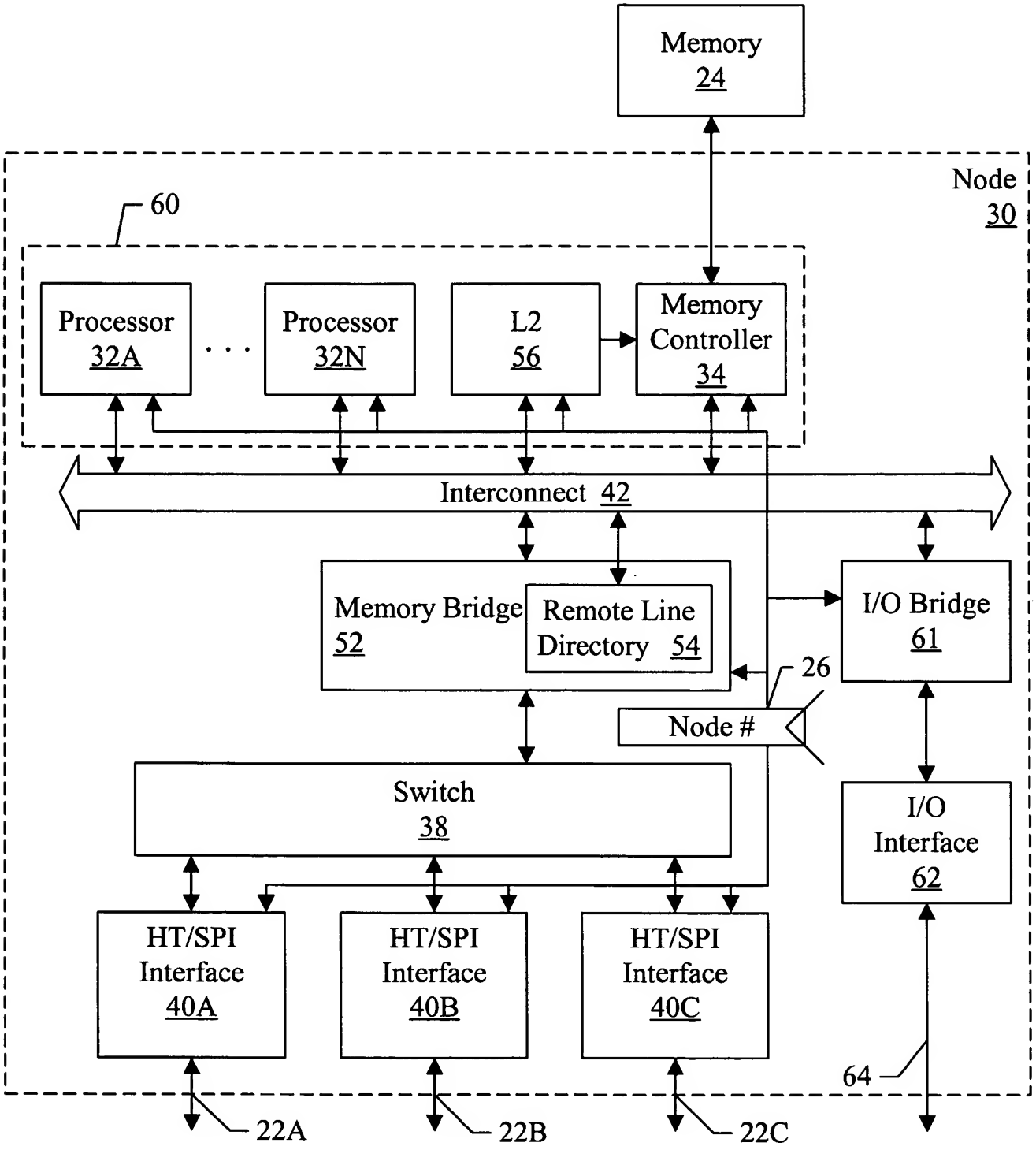
Memory
24
Node
30
60
Processor
32A
Processor
32N
L2
56
Memory
Controller
34
Interconnect 42
Memory Bridge
52
Remote Line
Directory 54
I/O Bridge
61
26
Node #
Switch
38
I/O
Interface
62
HT/SPI
Interface
40A
HT/SPI
Interface
40B
HT/SPI
Interface
40C
64
22A
22B
22C

Fig. 3

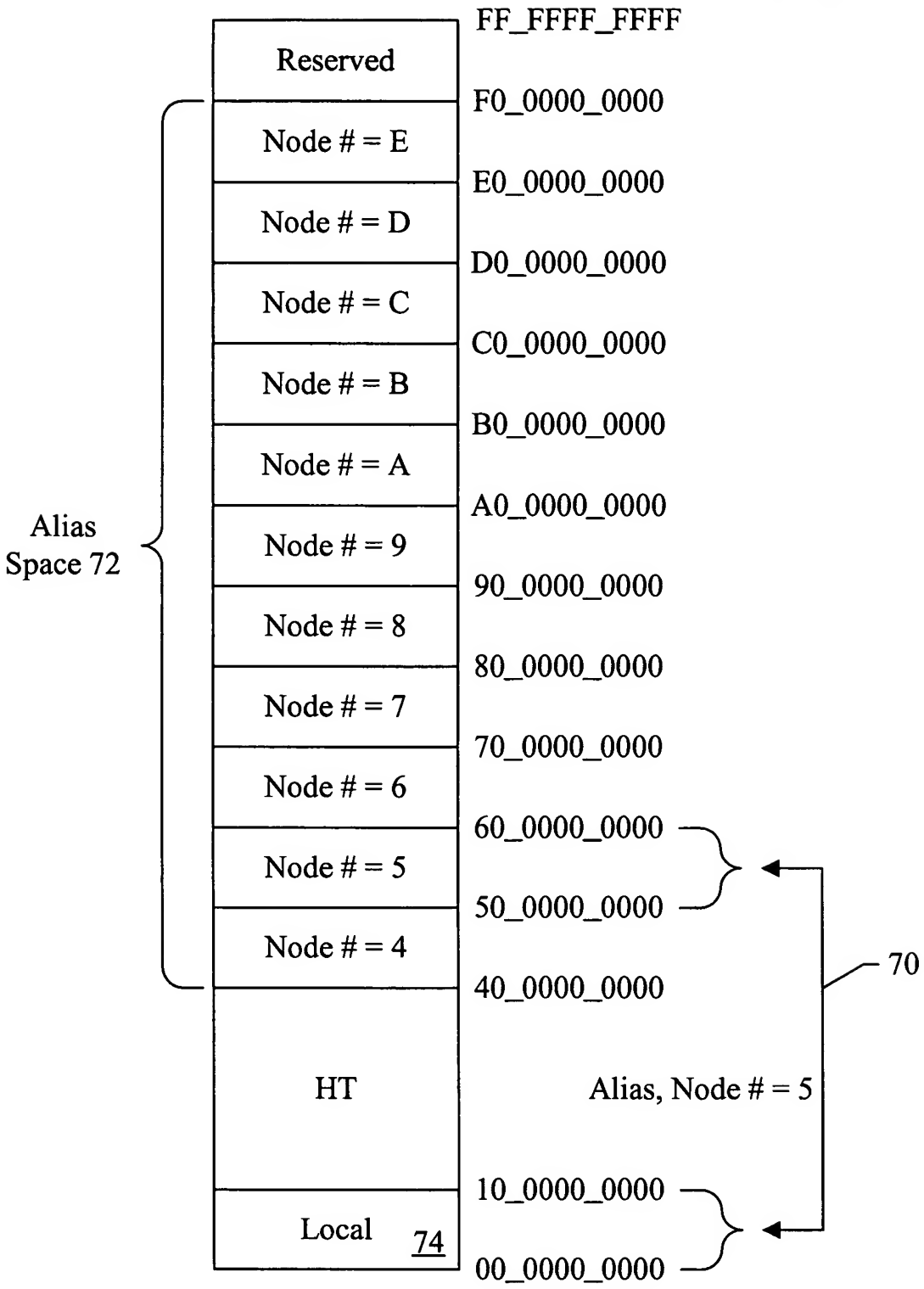
FF_FFFF_FFFF
Reserved
F0_0000_0000
Node # = E
E0_0000_0000
Node # = D
D0_0000_0000
Node # = C
C0_0000_0000
Node # = B
B0_0000_0000
Node # = A
A0_0000_0000
Node # = 9
90_0000_0000
Node # = 8
80_0000_0000
Node # = 7
70_0000_0000
Node # = 6
60_0000_0000
Node # = 5
50_0000_0000
Node # = 4
40_0000_0000
HT
Alias, Node # = 5
10_0000_0000
Local 74
00_0000_0000
Alias Space 72
70

Fig. 4

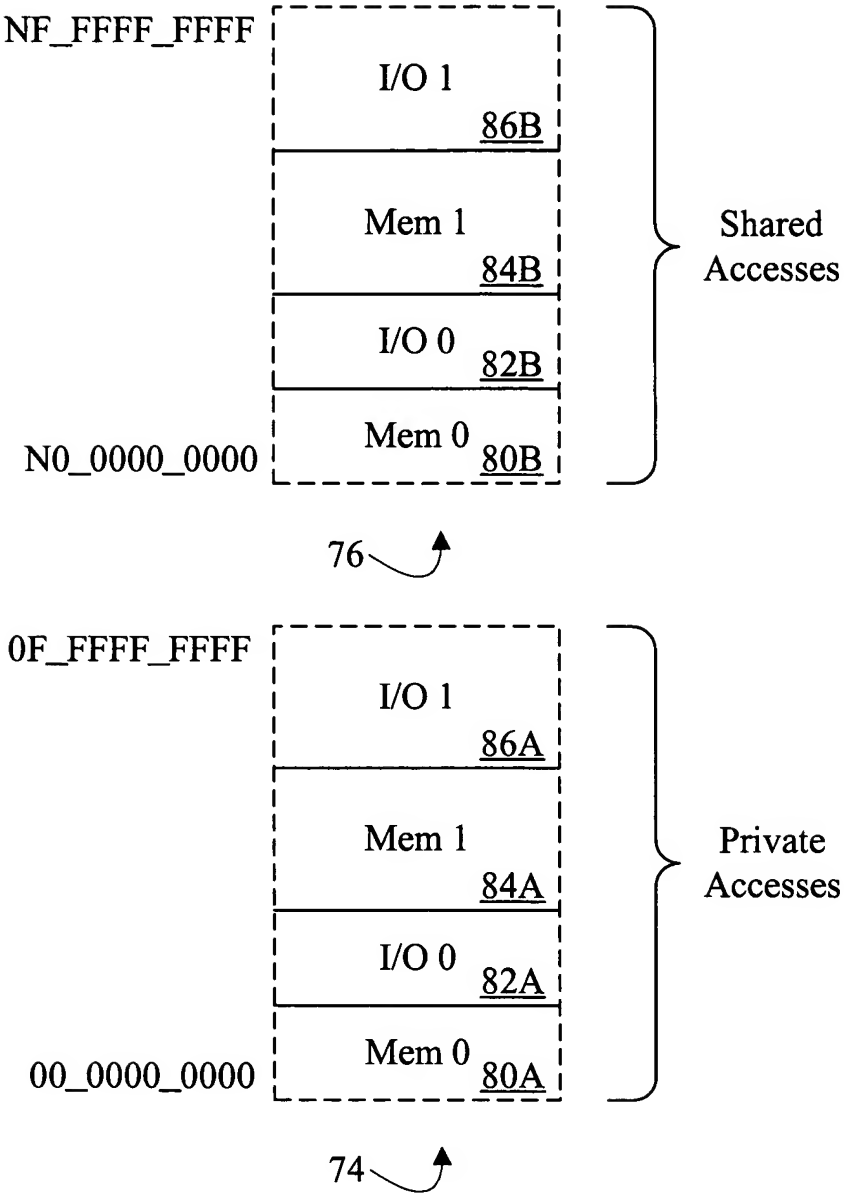
NF_FFFF_FFFF
I/O 1
86B
Mem 1
84B
I/O 0
82B
Mem 0
80B
N0_0000_0000
Shared
Accesses
76
0F_FFFF_FFFF
I/O 1
86A
Mem 1
84A
I/O 0
82A
Mem 0
80A
00_0000_0000
Private
Accesses
74

Fig. 5

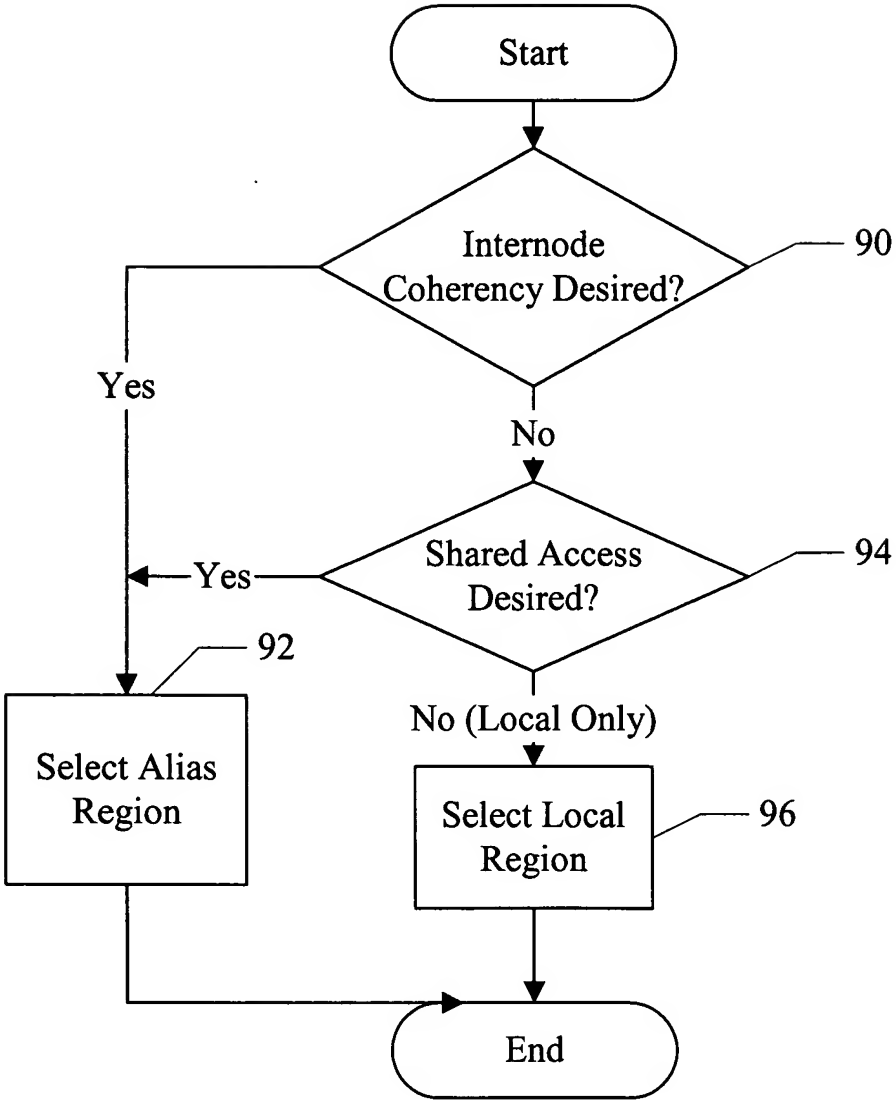
Start
Internode Coherency Desired?
90
Yes
No
Shared Access Desired?
94
Yes
92
Select Alias Region
No (Local Only)
Select Local Region
96
End

Fig. 6

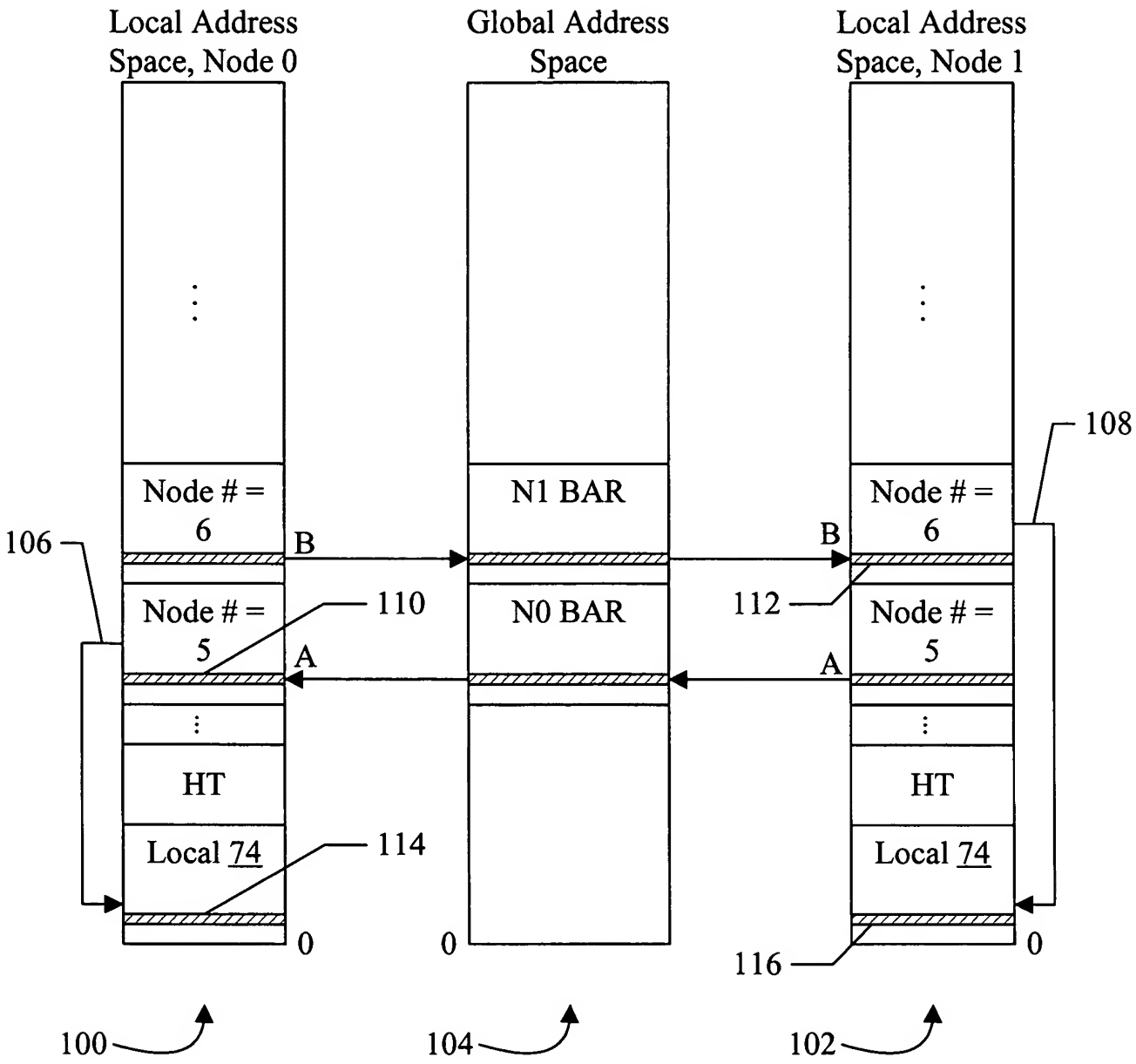
Local Address Space, Node 0
Global Address Space
Local Address Space, Node 1
Node # = 6
N1 BAR
Node # = 6
108
106
B
B
110
112
Node # = 5
N0 BAR
Node # = 5
A
A
HT
HT
Local 74
114
Local 74
0
0
116
0
100
104
102

Fig. 7

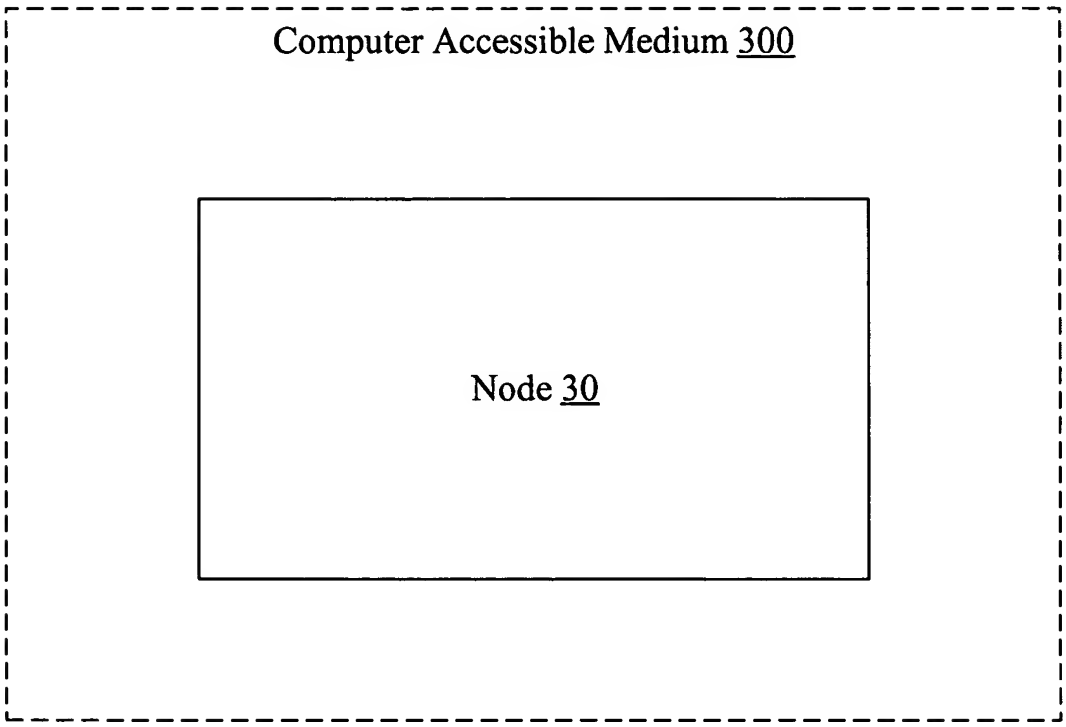

Fig. 8

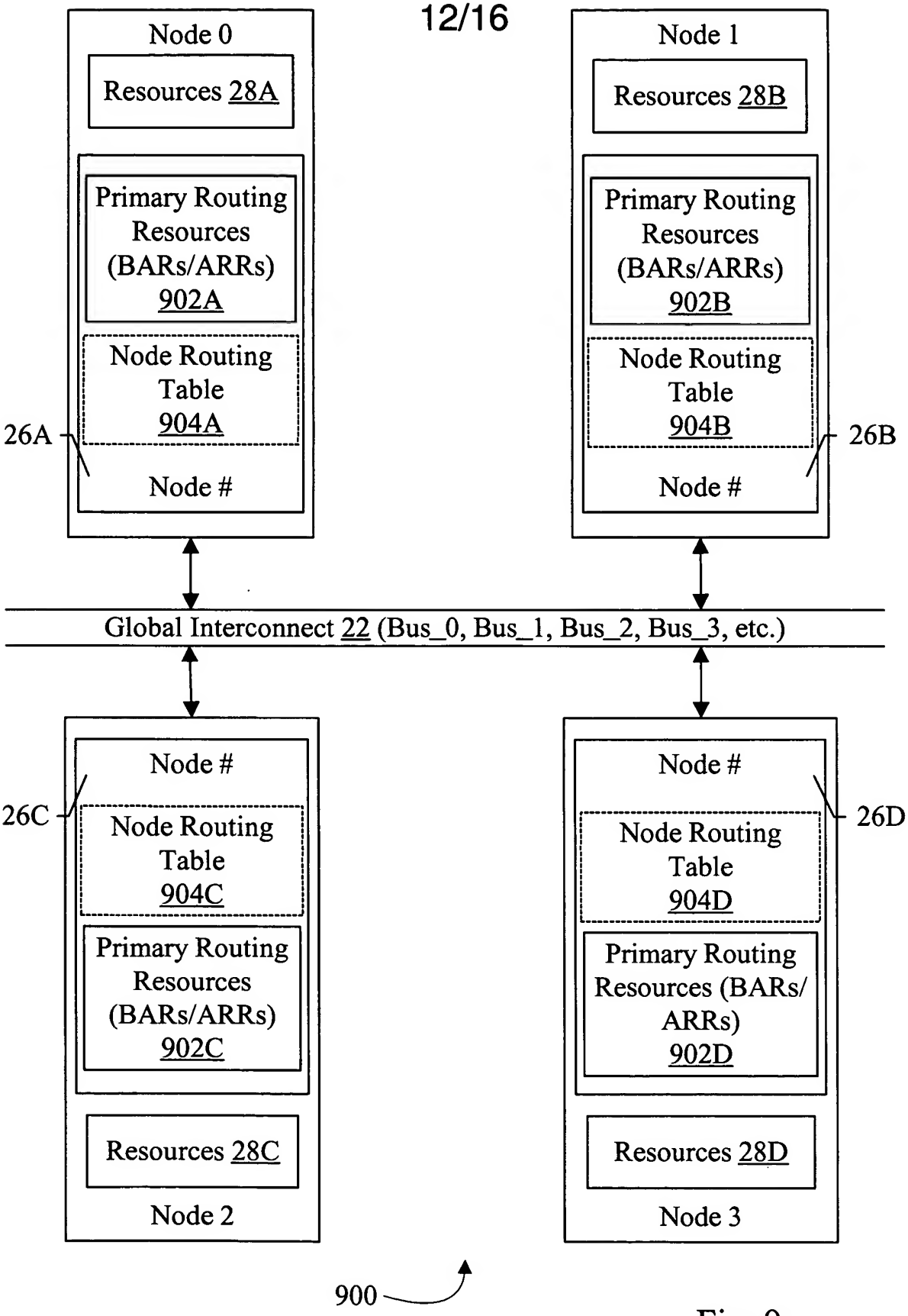
Node 0
Resources 28A
Primary Routing Resources (BARs/ARRs) 902A
Node Routing Table 904A
Node #
26A
Node 1
Resources 28B
Primary Routing Resources (BARs/ARRs) 902B
Node Routing Table 904B
Node #
26B
Global Interconnect 22 (Bus_0, Bus_1, Bus_2, Bus_3, etc.)
Node #
26C
Node Routing Table 904C
Primary Routing Resources (BARs/ARRs) 902C
Resources 28C
Node 2
Node #
26D
Node Routing Table 904D
Primary Routing Resources (BARs/ARRs) 902D
Resources 28D
Node 3
900

Fig. 9

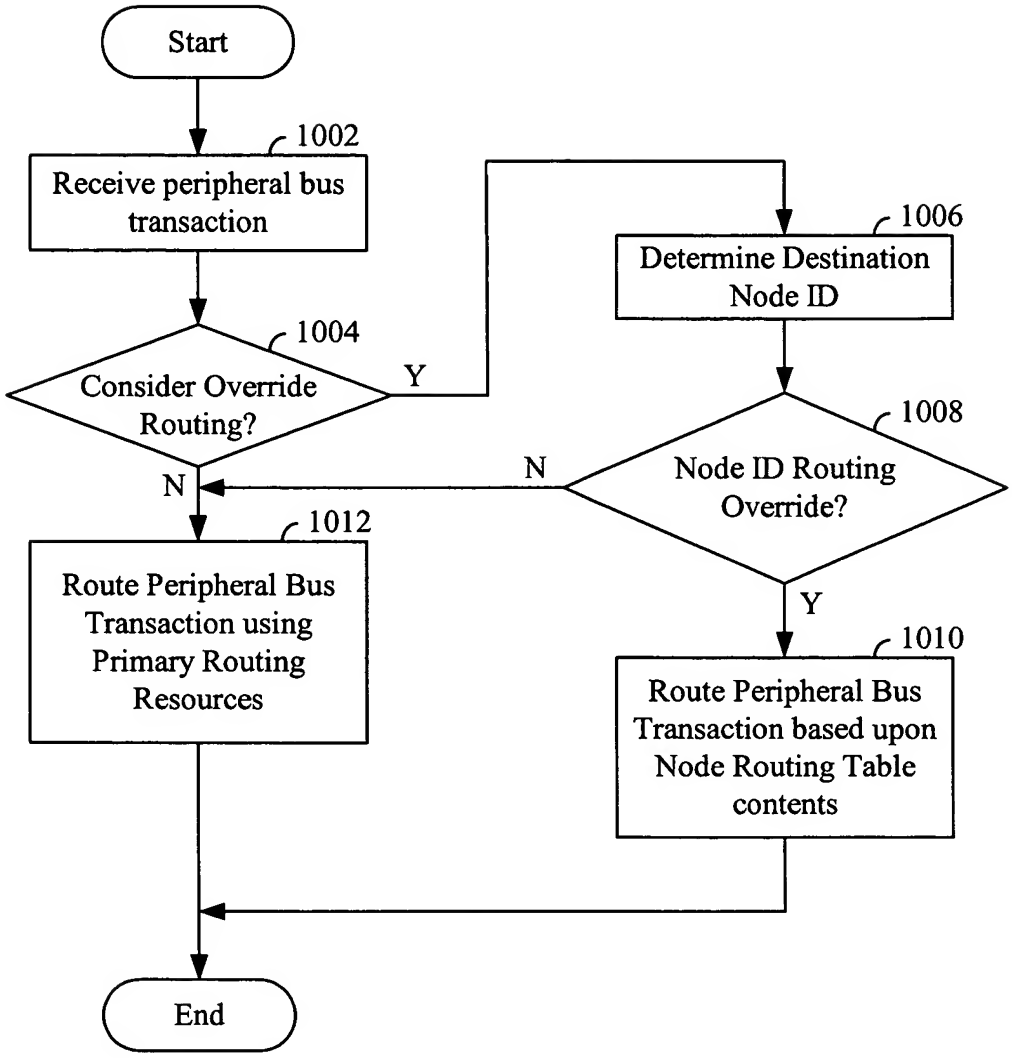
Start
1002
Receive peripheral bus transaction
1004
Consider Override Routing?
Y
N
1006
Determine Destination Node ID
1008
Node ID Routing Override?
N
Y
1012
Route Peripheral Bus Transaction using Primary Routing Resources
1010
Route Peripheral Bus Transaction based upon Node Routing Table contents
End

Fig. 10

Node Routing Table (Bridge A Entries) - 1100

MS-4 Addr. Bits					
0000	Node 0	I/O Override bit	P/S	CC Override bit	P/S
0001	Node 1	I/O Override bit	P/S	CC Override bit	P/S
0010	Node 2	I/O Override bit	P/S	CC Override bit	P/S
0011	Node 3	I/O Override bit	P/S	CC Override bit	P/S
0100	Node 4	I/O Override bit	P/S	CC Override bit	P/S
0101	Node 5	I/O Override bit	P/S	CC Override bit	P/S
0110	Node 6	I/O Override bit	P/S	CC Override bit	P/S
0111	Node 7	I/O Override bit	P/S	CC Override bit	P/S
1000	Node 8	I/O Override bit	P/S	CC Override bit	P/S
1001	Node 9	I/O Override bit	P/S	CC Override bit	P/S
1010	Node 10	I/O Override bit	P/S	CC Override bit	P/S
1011	Node 11	I/O Override bit	P/S	CC Override bit	P/S
1100	Node 12	I/O Override bit	P/S	CC Override bit	P/S
1101	Node 13	I/O Override bit	P/S	CC Override bit	P/S
1110	Node 14	I/O Override bit	P/S	CC Override bit	P/S
1111	Node 15	I/O Override bit	P/S	CC Override bit	P/S

Fig. 11

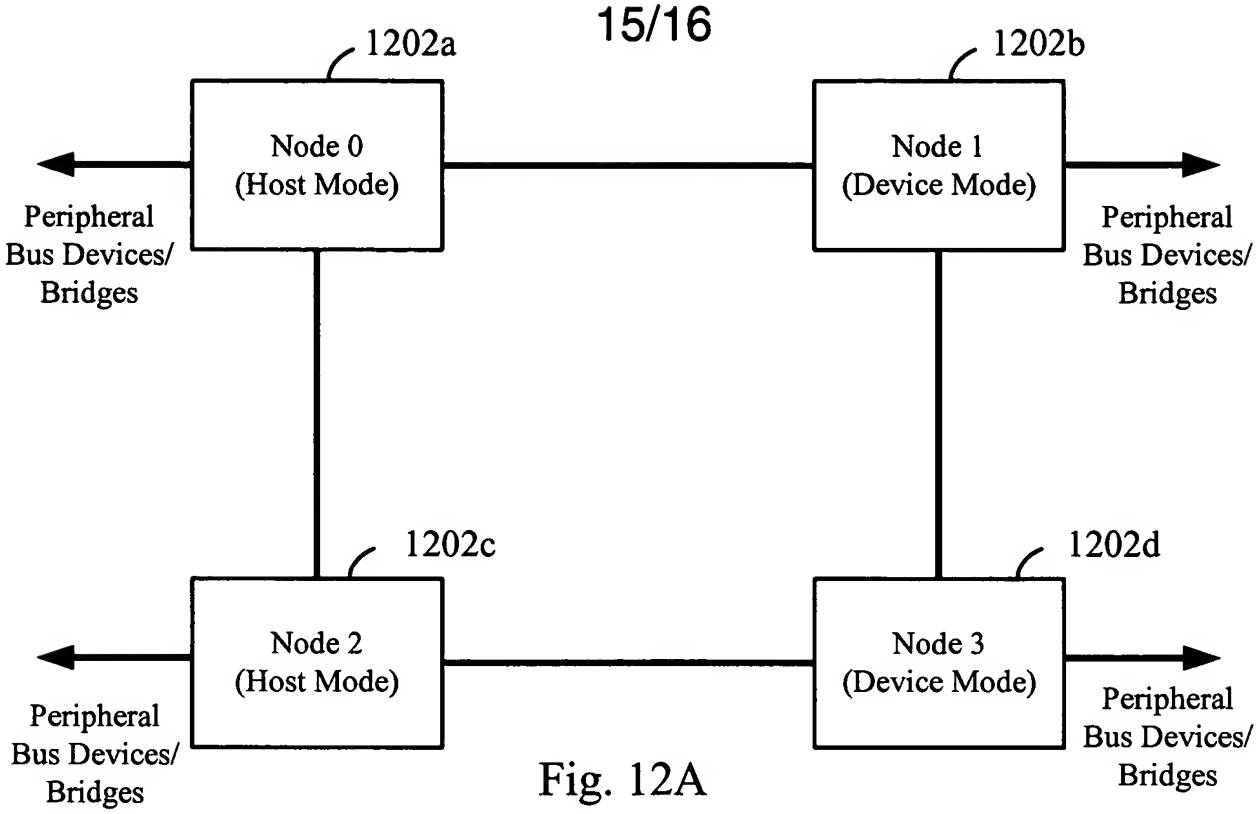

Fig. 12A

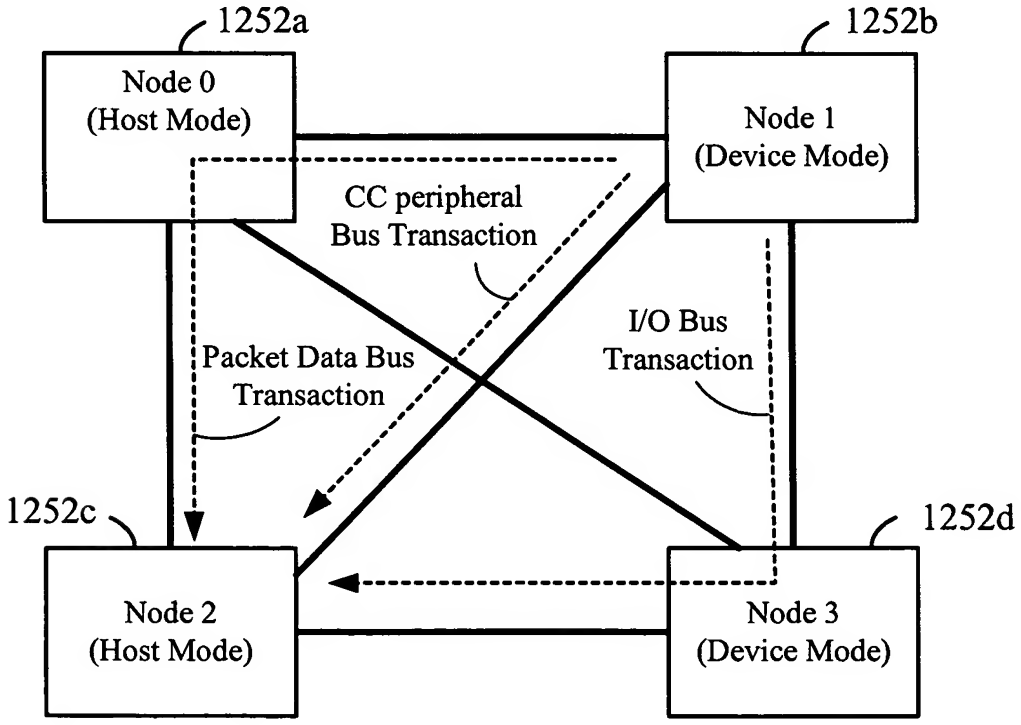

Fig. 12B

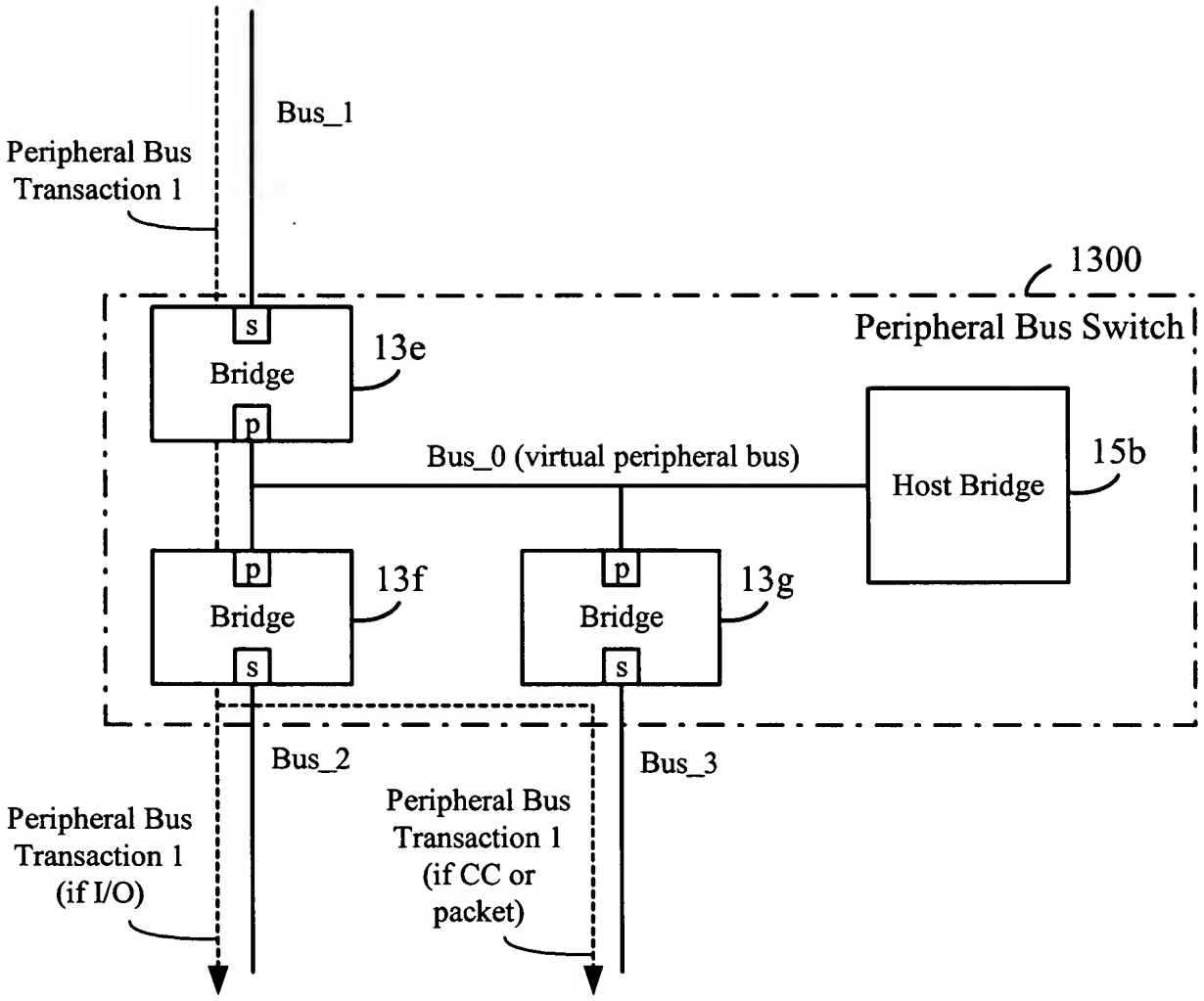
Bus_1
Peripheral Bus
Transaction 1
1300
Peripheral Bus Switch
s
Bridge
p
13e
Bus_0 (virtual peripheral bus)
Host Bridge
15b
p
Bridge
s
13f
p
Bridge
s
13g
Bus_2
Bus_3
Peripheral Bus
Transaction 1
(if I/O)
Peripheral Bus
Transaction 1
(if CC or
packet)

Fig. 13